Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A controller/driver comprising:

a work memory;

a graphic engine converting externally received image data into first bitmap data, and storing said first bitmap data into said work memory;

a display memory receiving and storing second bitmap data developed from said first bitmap data stored in said work memory; and

a driver circuit which receives said second bitmap data from said display memory, and drives a display panel in response to said second bitmap data received from said display memory,

~~wherein said work memory has first and second input ports, said first input port being connected to said graphic engine,~~

~~wherein said display memory has third and fourth input ports, said third input port being connected to said second input port, and said fourth input port being connected to a memory controller, and~~

~~wherein data transfer of said first bitmap data from said work memory to said display memory is performed such that a set of data bits of said first bitmap data are transferred at the same time,~~

wherein said first bitmap data includes a plurality of line data each including a plurality of pixel data associated with ~~a line of~~ respective pixels ~~of an image represented by said second bitmap data to be displayed on~~ associated with a corresponding gate line of said display panel, and

wherein said data transfer of said first bitmap data from said work memory to said display memory is ~~sequentially~~ performed such that each of said plurality of line data is transferred at the same time ~~in a horizontal period~~ in parallel from said work memory to said display memory.

2. (Original) The controller/driver according to claim 1, wherein said image data is described in a vector format.

3. (Previously Presented) The controller/driver according to claim 1, wherein said image data includes compressed image data.

4. (Canceled).

5. (Canceled).

6. (Previously Presented) The controller/driver according to claim 1, further comprising:

a latch receiving said line data from said work memory, and temporally storing said received line data.

7. (Previously Presented) The controller/driver according to claim 1, further comprising:

a timing controller controlling said work memory, said display memory, and said driver circuit so that said data transfer of said first bitmap data from said work memory to said display memory is synchronous with readout of said second bitmap data from said display memory to said driver circuit; and

a memory controller connected to said second input port of said work memory, said memory controller receiving bit map data from a processor for storage in said display memory.

8. (Original) The controller/driver according to claim 7, wherein said data transfer of said first bitmap data from said work memory to said display memory is initiated in response to activation of a frame synchronization signal indicating to start displaying each image frame.

9. (Previously Presented) The controller/driver according to claim 7, wherein said timing controller controls said display memory, and said driver circuit so that said data

transfer of said first bitmap data from said work memory to said display memory does not overrun said readout of said second bitmap data from said display memory to said driver circuit.

10. (Original) The controller/driver according to claim 1, wherein said work memory includes:

a plurality of first bit lines,

a plurality of first word lines, and

a plurality of first memory cells disposed at respective intersections of said first bit lines and first word lines to store therein said first bitmap data,

wherein said display memory includes:

a plurality of second bit lines,

a plurality of second word lines, and

a plurality of second memory cells disposed at respective intersections of said second bit lines and second word lines to store therein said second bitmap data,

wherein a number of said first bit lines is same as that of said second bit lines, and

wherein said first bit lines are connected to said second bit lines, respectively.

11. (Original) The controller/driver according to claim 10, wherein a number of said first word lines is identical to that of said second word lines.

12. (Previously Presented) The controller/driver according to claim 10, further comprising a timing controller controlling said work memory, and said display memory, and said driver circuit,

wherein said driver circuit is connected to said second bit lines, and

wherein said timing controller is adapted to deactivate said display memory to allow said first bitmap data to be transmitted from said work memory to said driver circuit through said second bit lines.

13. (Withdrawn – Previously Presented) The controller/driver according to claim 12, wherein said timing controller is adapted to successively change portions of said first and

second bitmap data stored in said work memory and said display memory to be transferred to said driver circuit.

14. (Withdrawn) The controller/driver according to claim 1, further comprising a processing circuit which processes said bitmap data received from said work memory to develop said bitmap data to be displayed and stores said developed bitmap data in said display memory.

15. (Withdrawn) The controller/driver according to claim 1, further comprising another processing circuit which processes said bitmap data stored in said display memory, and provides said processed bitmap data for said work memory.

16. (Withdrawn) A display device comprising:

a controller/driver; and

a first display panel including:

a plurality of first data lines, and

a plurality of first gate lines,

a second display panel including:

a plurality of second data lines respectively connected to said first data lines, and

a plurality of second gate lines,

wherein said controller driver includes:

a work memory comprising a plurality of first bit lines,

a graphic engine converting externally received image data into first bitmap data to store into said work memory,

a display memory storing a second bitmap data and comprising a plurality of second bit lines respectively connected to said first bit lines,

a data line driver driving said first data lines,

a first gate line driver driving said first gate lines,

a second gate line driver driving said second gate lines, and

a controller circuit controlling said work memory, said display memory, said data line driver, and said first and second gate line drivers,

wherein said controller circuit is adapted to deactivate said display memory to thereby allow said first bitmap data to be transmitted to said data line driver through said second bit lines, and to allow said second bitmap data to be transmitted from said display memory to said data line driver, and

wherein said controller circuit is adapted to control said first and second gate line drivers to allow said data line driver to drive said second data lines of said second display panel through said first data lines of said first display panel.

17. (Withdrawn) The display device according to claim 16, wherein said controller circuit is adapted said first and second gate line drivers to allow the same image to be displayed on said first and second display panels in response to one of said first and second bitmap data.

18 (Canceled).

19. (Previously Presented) The controller/driver according to claim 1, further comprising:

a latch receiving said first bitmap data from said work memory, and temporally storing said first bitmap data; and

a timing controller for controlling output of data from said latch,

wherein said display memory receives said first bitmap data output from said latch,

wherein said work memory and said display memory are operated at different times due to having said latch provided therebetween.

20. (Previously Presented) The controller/driver according to claim 1, further comprising:

means for transferring said first bitmap data from said work memory to said display memory; and

means for displaying said second bitmap data output from said display memory on said display panel,

wherein a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel.